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**Cogent CSB1701
CSB17xx Network SOM
Development Board**

**Hardware Reference Manual
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1 WARRANTY

The enclosed product ("the Product"), a part of the Cogent Modular Architecture or Cogent Single Board series, is warranted by Cogent Computer Systems, Inc. ("Cogent") for a period of six months for reasonable development testing and use, all as further described and defined below. This warranty runs solely to the individual or entity purchasing the Product and is not transferable or assignable in any respect. This warranty is valid only for so long as the product is used intact as shipped from Cogent. Any attempt or effort to alter the Product, including but not limited to any attempt to solder, de-solder, unplug, replace, add or affix any part or component of or onto the Product, other than components specifically intended for the user to plug and unplug into appropriate sockets and/or connectors to facilitate user programming and development, all as specifically described and authorized in the Cogent Customer Product Users Manual, shall void this warranty in all respects. Coverage under this warranty requires that the Product be used and stored at all times in conditions with proper electrostatic protection necessary and appropriate for a complex electronic device. These conditions include proper temperature, humidity, radiation, atmosphere and voltage (standard commercial environment, 0C to +70C, <60%RH). Any Product that has been modified without the express, prior written consent of Cogent is not covered by this warranty. Cogent Single Board and Cogent Modular Architecture test and bus connectors are for use with Cogent adapters only. The use or connection of any test or bus connector, adapter or component with any device other than a Cogent connector or adapter shall void this warranty and the warranty of all other components, parts and modules connected to the rest of the system. Cogent shall not be responsible for any damage to the Product as a result of a customer's use or application of circuitry not developed or approved by Cogent for use on or in connection with the Product.

This warranty does not cover defects caused by electrical or temperature fluctuations or from stress resulting from or caused by abuse, misuse or misapplication of the Product. Any evidence of tampering with the serial number on the Product shall immediately void this warranty. This Product is not intended to be used on or embedded in or otherwise used in connection with any life sustaining or life saving product and this warranty is not applicable nor is Cogent liable in any respect if the Product is so used. Notwithstanding anything to the contrary herein, Cogent expressly disclaims any implied warranty of merchantability or implied warranty of fitness for a particular purpose in connection with the manufacture or use of the Product.

2 OVERVIEW

2.1 INTRODUCTION

The CSB1701 was designed and developed by Cogent Computer Systems, Inc. as a Hardware and Software development platform for the CSB17xx series MXM Network SOM's (System On a Module). The CSB1701 provides the CSB17xx developer access to the CSB17xx signals as well as a complete set of features required for software development and hardware expansion.

2.2 CSB1701 FEATURES

- **PCI EXPRESS SOCKET 1** - This x16 Socket is connected to SOM PCI Express Port 0, Lanes 0-3. The actual width (x1, x2 or x4) is SOM specific.
- **PCI EXPRESS SOCKET 2** - This x1 Socket is connected to SOM PCI Express Port 1.
- **PCI EXPRESS SOCKET 3** - This x1 Socket is connected to SOM PCI Express Port 2.
- **10/100/1000 ETHERNET** - Two Shielded, Combo Dual USB/RJ45 Connectors with Magnetics provide access to the SOM Copper Ethernet Ports. They are compatible with both 10/100 and Gigabit SOM's.
- **SGMII/XAUI SERDES** - An offset mounted PCIe x4 Connector is used to provide access to SOM SGMII Ports 2-5 or XAUI.
- **SATA** - Two Standard 7-Pin SATA Connectors allow access to SOM SATA Ports 0 and 1.
- **REMOTE LCD I/F** - A high speed Mini-SAS Connector provides access to the SOM LVDS. It also brings out SOM USB Host Port 1 for HMI applications.
- **SD/MMC SOCKET** - A full size SD/MMC socket provides access to the SOM SD/MMC Port.
- **HIGH SPEED USB HUB** - SOM USB Host port 0 goes to a Four Port High Speed USB Hub. Ports 0 and 1 of this Hub go to Combo Ethernet/USB Jack 0, while ports 2 and 3 go to Combo Ethernet/USB Jack 1. SOM USB Host Port 1 goes to the Remote Display I/F Connector.
- **CONSOLE I/O** - UART0 is converted to USB and accessed via a Mini-B Connector.
- **CPU SPECIFIC I/O HEADERS** - A 40-Pin Header provides access to the CPU Specific I/O Ports: UART1; UART2/CAN; TDM/SSP; I2S/AC97; SPI; and I2C.
- **JTAG** - A 20-Pin Header provides access to the CPU JTAG Port.
- **COGENT MXM SOM SUPPORT** - Common, Interchangeable Footprint across Multiple CPU Architectures; Supports MXM SOM A-Size (50mm x 70mm), B-Size (75mm x 70mm) and C-Size (100mm x 70mm), Network Pinout; 12V Fan Header controlled by SOM IPM Micro for Active CPU Cooling; plus 8-Position DIP Switch for SOM Configuration Options.
- **POWER SUPPLY** - 24-Pin ATX Power Supply Connector (SOM uses +12V only)
- **FLEX-ATX SIZE** - 170mm x 228.6mm (7.5" x 9.0") Board fits into almost any off the shelf Micro-ATX Enclosure including Small Form Factor (SFF) Enclosures.

2.3 BLOCK DIAGRAM

Refer to the following figure for a block diagram of the CSB1701.

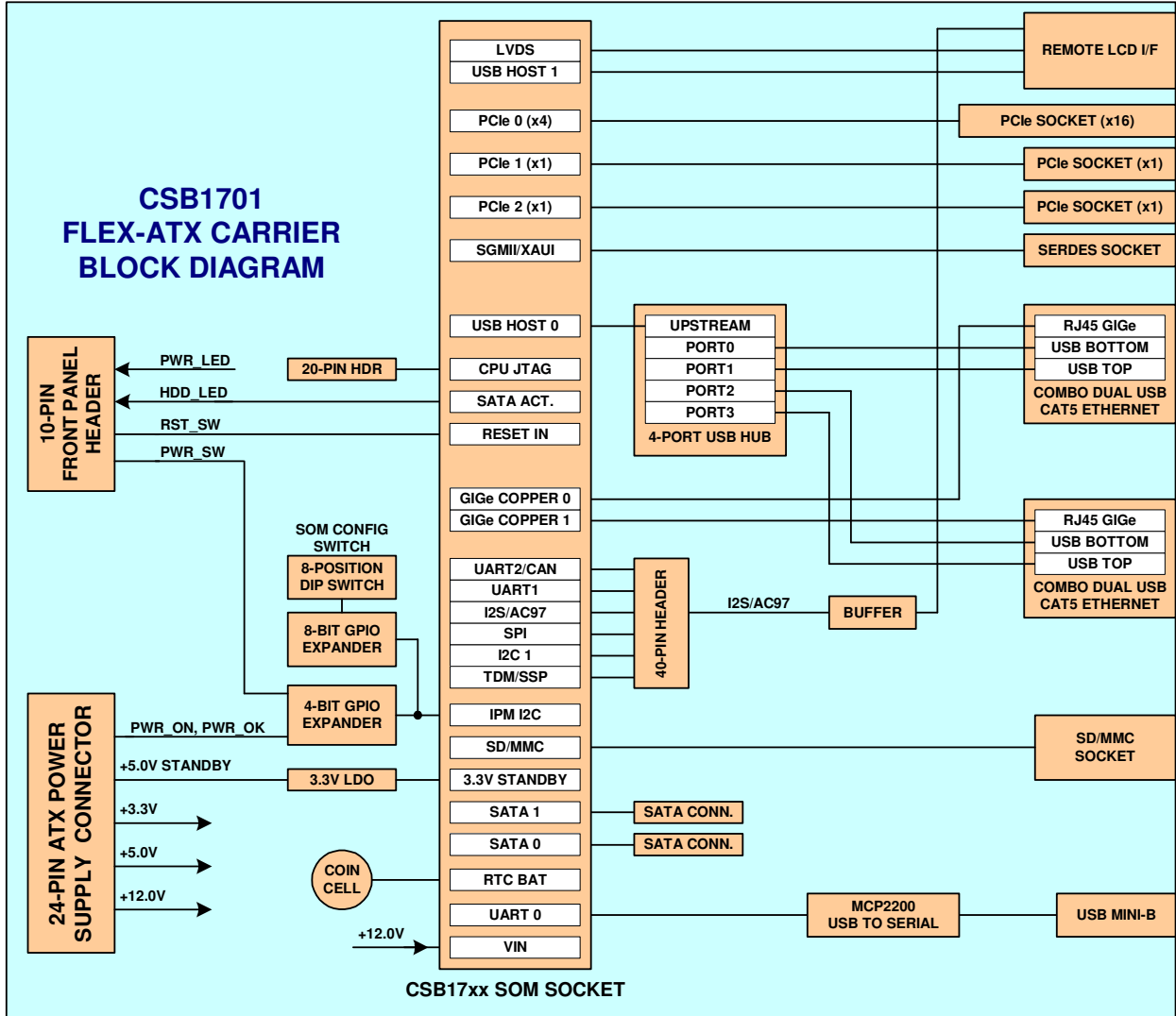


Figure 1 – CSB1701 Block Diagram

3 CSB17XX SOM CONNECTOR

3.1 OVERVIEW

This section describes the connector used to mount the CSB17xx SOM to the CSB1701. It includes a pin-out table and detailed signal descriptions.

3.2 CSB17XX MXM CONNECTOR DESCRIPTION

The CSB1701 is fully compatible with the Cogent CSB17xx family of Cogent MXM SOM (System On a Module) boards. The CSB17xx family uses the low cost, high performance MXM II connector originally developed for laptop computer graphics cards. However, the Cogent MXM SOM form factor, pinout and pin orientation are not related to, nor compatible with, any other form factor.

3.3 CSB17XX MXM CONNECTOR PINOUT

The following table lists the pinout and signal descriptions of the CSB17xx MXM Connector. Pins labeled “Axx” are located on the top side of the SOM while those labeled “Bxx” are on the bottom. The pin assignments conform to the “NETWORK” variant of the CSB17xx MXM SOM family. Please refer to the appropriate CSB17xx MXM Network SOM HW Reference Manual for detailed information on the supported signals.

PIN	NAME	DESCRIPTION	CSB1701 USAGE
A1	GE0_MDI_0_M	GIGE 0 MDI 0 MINUS	USB/RJ45 JACK P7, Pin 2
B1	*GE1_SPD1G	GIGE 1 SPEED 1GBIT LED	USB/RJ45 JACK P20, Pin 13
A2	GE0_MDI_0_P	GIGE 0 MDI 0 PLUS	USB/RJ45 JACK P7, Pin 3
B2	*GE0_SPD1G	GIGE 0 SPEED 1GBIT LED	USB/RJ45 JACK P7, Pin 13
A3	GE0_MDI_1_M	GIGE 0 MDI 1 MINUS	USB/RJ45 JACK P7, Pin 4
B3	*GE1_LNK	GIGE 1 LINK/ACTIVITY	USB/RJ45 JACK P20, Pin 11
A4	GE0_MDI_1_P	GIGE 0 MDI 1 PLUS	USB/RJ45 JACK P7, Pin 5
B4	*GE0_LNK	GIGE 0 LINK/ACTIVITY	USB/RJ45 JACK P7, Pin 11
A5	VCC3	3.3V OUTPUT	
B5	VCC3	3.3V OUTPUT	
A6	GE0_MDI_2_M	GIGE 0 MDI 2 MINUS	USB/RJ45 JACK P7, Pin 6
B6	*GE1_SPD100	GIGE 1 SPEED 100MBIT LED	USB/RJ45 JACK P20, Pin 14
A7	GE0_MDI_2_P	GIGE 0 MDI 2 PLUS	USB/RJ45 JACK P7, Pin 7
B7	*GE0_SPD100	GIGE 0 SPEED 100MBIT LED	USB/RJ45 JACK P7, Pin 14
A8	GE0_MDI_3_M	GIGE 0 MDI 3 MINUS	USB/RJ45 JACK P7, Pin 8

PIN	NAME	DESCRIPTION	CSB1701 USAGE
B8	MDIO	MII BUS DATA FOR EXTERNAL PHYS	SERDES Connector P9, Pin A6
A9	GE0_MDI_3_P	GIGE 0 MDI 3 PLUS	USB/RJ45 JACK P7, Pin 9
B9	MDC	MII BUS CLOCK FOR EXTERNAL PHYS	SERDES Connector P9, Pin A5
A10	GE1_MDI_3_M	GIGE 1 MDI 3 MINUS	USB/RJ45 JACK P7, Pin 9
B10	*MII_INT	MII BUS INTERRUPT FROM EXTERNAL PHYS	SERDES Connector P9, Pin A7
A11	GE1_MDI_3_P	GIGE 1 MDI 3 PLUS	USB/RJ45 JACK P20, Pin 8
B11	*I2C_INT	SHARED I2C BUS INTERRUPT	SOM I/O Header P10, Pin 8 SERDES Connector P9, Pin B11 Remote Display I/F Connector P8, Pin A17
A12	GE1_MDI_2_M	GIGE 1 MDI 2 MINUS	USB/RJ45 JACK P20, Pin 7
B12	I2C0_SCL	PRIMARY I2C BUS CLOCK	SOM I/O Header P10, Pin 6
A13	GE1_MDI_2_P	GIGE 1 MDI 2 PLUS	USB/RJ45 JACK P20, Pin 6
B13	I2C0_SDA	PRIMARY I2C BUS DATA	SOM I/O Header P10, Pin 7
A14	GND	GROUND	
B14	GND	GROUND	
A15	GE1_MDI_1_M	GIGE 1 MDI 1 MINUS	USB/RJ45 JACK P20, Pin 5
B15	GE_CTREF	GIGE CENTER TAP REFERENCE VOLTAGE	USB/RJ45 JACK P7, Pin 1 USB/RJ45 JACK P20, Pin 1
A16	GE1_MDI_1_P	GIGE 1 MDI 1 PLUS	USB/RJ45 JACK P20, Pin 4
B16	GE_CTREF	SAME AS B15	Same as B15
A17	GE1_MDI_0_M	GIGE 1 MDI 0 MINUS	USB/RJ45 JACK P20, Pin 3
B17	I2C1_SCL	SECONDARY I2C BUS CLOCK	SOM I/O Header P10, Pin 6 Remote Display I/F Connector P8, Pin A10
A18	GE1_MDI_0_P	GIGE 1 MDI 0 PLUS	USB/RJ45 JACK P20, Pin 2
B18	I2C1_SDA	SECONDARY I2C BUS DATA	SOM I/O Header P10, Pin 7 Remote Display I/F Connector P8, Pin A11
A19	VCC3	3.3V OUTPUT	
B19	VCC3	3.3V OUTPUT	
A20	SG1_TD_M	SGMII 1 TRANSMIT MINUS	Unconnected
B20	SG1_RD_M	SGMII 1 RECEIVE MINUS	Unconnected
A21	SG1_TD_P	SGMII 1 TRANSMIT PLUS	Unconnected
B21	SG1_RD_P	SGMII 1 RECEIVE PLUS	Unconnected

PIN	NAME	DESCRIPTION	CSB1701 USAGE
A22	SG1_SD	SGMII 1 SIGNAL DETECT	Unconnected
B22	SG0_SD	SGMII 0 SIGNAL DETECT	Unconnected
A23	SG0_TD_M	SGMII 0 TRANSMIT MINUS	Unconnected
B23	SG0_RD_M	SGMII 0 RECEIVE MINUS	Unconnected
A24	SG0_TD_P	SGMII 0 TRANSMIT PLUS	Unconnected
B24	SG0_RD_P	SGMII 0 RECEIVE PLUS	Unconnected
A25	GND	GROUND	
B25	GND	GROUND	
A26	SA1_TD_M	CPU SATA 1 TRANSMIT MINUS	SATA Connector P13, Pin 3
B26	SA1_RD_M	CPU SATA 1 RECEIVE MINUS	SATA Connector P13, Pin 2
A27	SA1_TD_P	CPU SATA 1 TRANSMIT PLUS	SATA Connector P13, Pin 5
B27	SA1_RD_P	CPU SATA 1 RECEIVE PLUS	SATA Connector P13, Pin 6
A28	*SA1_ACT	SATA 1 ACTIVITY	RED LED D13 and Front Panel Header P4, Pin 3
B28	*SA0_ACT	SATA 0 ACTIVITY	RED LED D13 and Front Panel Header P4, Pin 3
A29	SA0_TD_M	CPU SATA 0 TRANSMIT MINUS	SATA Connector P14, Pin 3
B29	SA0_RD_M	CPU SATA 0 RECEIVE MINUS	SATA Connector P14, Pin 2
A30	SA0_TD_P	CPU SATA 0 TRANSMIT PLUS	SATA Connector P14, Pin 5
B30	SA0_RD_P	CPU SATA 0 RECEIVE PLUS	SATA Connector P14, Pin 6
A31	VCC3	3.3V OUTPUT	
B31	VCC3	3.3V OUTPUT	
A32	UH1_M	USB HOST PORT 1 MINUS	Remote Display I/F Connector P8, Pin A14
B32	UH0_M	USB HOST PORT 0 MINUS	USB2514 HUB, Pin 30 (USBUP_DM)
A33	UH1_P	USB HOST PORT 1 PLUS	Remote Display I/F Connector P8, Pin A13
B33	UH0_P	USB HOST PORT 0 PLUS	USB2514 HUB, Pin 31 (USBUP_DP)
A34	GND	GROUND	
B34	GND	GROUND	
A35	VGA_R	ANALOG VGA RED	Unconnected
B35	VGA_HS	ANALOG VGA HORIZONTAL SYNC	Unconnected
A36	VGA_G	ANALOG VGA GREEN	Unconnected
B36	VGA_VS	ANALOG VGA VERTICAL SYNC	Unconnected

PIN	NAME	DESCRIPTION	CSB1701 USAGE
A37	VGA_B	ANALOG VGA BLUE	Unconnected
B37	I2S_MCLK	I2S MASTER CLOCK	SOM I/O Header P10, Pin 10 and Remote Display I/F Connector P8, Pin B8
A38	TDM_RFS/ *TDM_INT	TDM RECEIVE FRAME SYNC OR TDM INTERRUPT	SOM I/O Header P10, Pin 11
B38	TDM_RCK/ *TDM_RST	TDM RECEIVE CLOCK OR TDM RESET	SOM I/O Header P10, Pin 12
A39	VCC3	3.3V OUTPUT	
B39	VCC3	3.3V OUTPUT	
A40	MC_CLK	SD/MMC CLOCK	SD/MMC Socket SD1, Pin 5
B40	MC_CS_D3	SD/MMC DATA 3 (SPI CS)	SD/MMC Socket SD1, Pin 1
A41	MC_DIN_CMD	SD/MMC COMMAND (SPI MOSI)	SD/MMC Socket SD1, Pin 2
B41	MC_DOUT_D0	SD/MMC DATA 0 (SPI MISO)	SD/MMC Socket SD1, Pin 7
A42	MC_IRQ_D1	SD/MMC DATA 1 (SPI/SDIO IRQ)	SD/MMC Socket SD1, Pin 8
B42	MC_D2	SD/MMC DATA 2	SD/MMC Socket SD1, Pin 9
A43	MC_WP	SD/MMC WRITE PROTECT	SD/MMC Socket SD1, Pin 12
B43	*MC_CD	SD/MMC DETECT	SD/MMC Socket SD1, Pin 10
A44	GND	GROUND	
B44	GND	GROUND	
A45	I2S_BCLK	I2S BIT CLOCK	SOM I/O Header P10, Pin 15 and Remote Display I/F Connector P8, Pin B9
B45	I2S_LRCLK	I2S LEFT/RIGHT CLOCK	SOM I/O Header P10, Pin 16 and Remote Display I/F Connector P8, Pin B10
A46	I2S_SDOUT	I2S SERIAL DATA OUT	SOM I/O Header P10, Pin 17 Remote Display I/F Connector P8, Pin B11
B46	I2S_SDIN	I2S SERIAL DATA IN	SOM I/O Header P10, Pin 18
A47	SSI_CLK/ TDM_CLK	SSI CLOCK OR TDM CLOCK	SOM I/O Header P10, Pin 23
B47	SSI_SYNC/ TDM_FS	SSI FRAME SYNEC OR TDM FRAME SYNC	SOM I/O Header P10, Pin 24
A48	SSI_TXD/ TDM_TXD	SSI TRANSMIT DATA OR TDM TRANSMIT DATA	SOM I/O Header P10, Pin 21
B48	SSI_RXD/ TDM_RXD	SSI RECEIVE DATA OR TDM RECEIVE DATA	SOM I/O Header P10, Pin 22
A49	VCC3	3.3V OUTPUT	

PIN	NAME	DESCRIPTION	CSB1701 USAGE
B49	VCC3	3.3V OUTPUT	
A50	SPI_CLK	SPI CLOCK	SOM I/O Header P10, Pin 27
B50	*SPI_CS	SPI CHIP SELECT	SOM I/O Header P10, Pin 28
A51	SPI_MOSI	SPI MASTER OUT/SLAVE IN	SOM I/O Header P10, Pin 23
B51	SPI_MISO	SPI MASTER IN/SLAVE OUT	SOM I/O Header P10, Pin 26
A52	U2_TXD	UART 2 TRANSMIT	SOM I/O Header P10, Pin 31
B52	U2_RXD	UART 2 RECEIVE	SOM I/O Header P10, Pin 32
A53	U2_RTS	UART 2 REQUEST TO SEND	SOM I/O Header P10, Pin 33
B53	U2_CTS	UART 2 CLEAR TO SEND	SOM I/O Header P10, Pin 34
A54	GND	GROUND	
B54	GND	GROUND	
A55	U1_TXD	UART 1 TRANSMIT	SOM I/O Header P10, Pin 35
B55	U1_RXD	UART 1 RECEIVE	SOM I/O Header P10, Pin 36
A56	U1_RTS	UART 1 REQUEST TO SEND	SOM I/O Header P10, Pin 37
B56	U1_CTS	UART 1 CLEAR TO SEND	SOM I/O Header P10, Pin 38
A57	U0_TXD	UART 0 TRANSMIT	MCP220 USB to Serial, Pin 12 (RXD)
B57	U0_RXD	UART 0 RECEIVE	MCP220 USB to Serial, Pin 19 (TXD)
A58	U0_RTS	UART 0 CLEAR TO SEND	MCP220 USB to Serial, Pin 13 (RTS)
B58	U0_CTS	UART 0 REQUEST TO SEND	MCP220 USB to Serial, Pin 11 (CTS)
A59	VCC3	3.3V OUTPUT	
B59	VCC3	3.3V OUTPUT	
A60	*RST_IN	SOM RESET IN	SOM JTAG Header P2, Pin 15 Front Panel Header P4, Pin 5 Pushbutton Switch SW2
B60	*RST_OUT	SOM RESET OUT	PCIe Socket P18, Pin A11 PCIe Socket P16, Pin A11 PCIe Socket P17, Pin A11 SERDES Connector P9, Pin A11 SOM I/O Header P10, Pin 5
A61	*TRST	JTAG RESET	SOM JTAG Header P2, Pin 3
B61	TCK	JTAG CLOCK	SOM JTAG Header P2, Pin 9
A62	TMS	JTAG MODE	SOM JTAG Header P2, Pin 7
B62	TDI	JTAG DATA IN	SOM JTAG Header P2, Pin 5

PIN	NAME	DESCRIPTION	CSB1701 USAGE
A63	TDO	JTAG DATA OUT	SOM JTAG Header P2, Pin 13
B63	DBG0	DEBUG SIGNAL 0	SOM Debug Header P3, Pin 1
A64	DBG1	DEBUG SIGNAL 1	SOM Debug Header P3, Pin 3
B64	DBG2	DEBUG SIGNAL 2	SOM Debug Header P3, Pin 5
A65	GND	GROUND	
B65	GND	GROUND	
A66	SD3_TD_M	CPU SERDES 3 TRANSMIT MINUS	SERDES Connector P9, Pin A16
B66	SD3_RD_M	CPU SERDES 3 RECEIVE MINUS	SERDES Connector P9, Pin B14
A67	SD3_TD_P	CPU SERDES 3 TRANSMIT PLUS	SERDES Connector P9, Pin A17
B67	SD3_RD_P	CPU SERDES 3 RECEIVE PLUS	SERDES Connector P9, Pin B15
A68	SD3_IO	CPU SERDES 3 I/O	SERDES Connector P9, Pin B12
B68	SD2_IO	CPU SERDES 2 I/O	SERDES Connector P9, Pin A19
A69	SD2_TD_M	CPU SERDES 2 TRANSMIT MINUS	SERDES Connector P9, Pin A21
B69	SD2_RD_M	CPU SERDES 2 RECEIVE MINUS	SERDES Connector P9, Pin B19
A70	SD2_TD_P	CPU SERDES 2 TRANSMIT PLUS	SERDES Connector P9, Pin A22
B70	SD2_RD_P	CPU SERDES 2 RECEIVE PLUS	SERDES Connector P9, Pin B20
A71	VCC3	3.3V OUTPUT	
B71	VCC3	3.3V OUTPUT	
A72	SD1_TD_M	CPU SERDES 1 TRANSMIT MINUS	SERDES Connector P9, Pin A25
B72	SD1_RD_M	CPU SERDES 1 RECEIVE MINUS	SERDES Connector P9, Pin B23
A73	SD1_TD_P	CPU SERDES 1 TRANSMIT PLUS	SERDES Connector P9, Pin A26
B73	SD1_RD_P	CPU SERDES 1 RECEIVE PLUS	SERDES Connector P9, Pin B24
A74	SD1_IO	CPU SERDES 1 I/O	SERDES Connector P9, Pin B30
B74	SD0_IO	CPU SERDES 0 I/O	SERDES Connector P9, Pin A32
A75	SD0_TD_M	CPU SERDES 0 TRANSMIT MINUS	SERDES Connector P9, Pin A29
B75	SD0_RD_M	CPU SERDES 0 RECEIVE MINUS	SERDES Connector P9, Pin B27
A76	SD0_TD_P	CPU SERDES 0 TRANSMIT PLUS	SERDES Connector P9, Pin A30
B76	SD0_RD_P	CPU SERDES 0 RECEIVE PLUS	SERDES Connector P9, Pin B28
A77	GND	GROUND	
B77	GND	GROUND	
A78	REF_CLK_M	PCIe REFERENCE CLOCK MINUS	PCIe Clock Generator U9

PIN	NAME	DESCRIPTION	CSB1701 USAGE
B78	SD_CLK_M	SERDES REFERENCE CLOCK MINUS	SERDES Connector, Pin A14
A79	REF_CLK_P	PCIe REFERENCE CLOCK PLUS	PCIe Clock Generator U9
B79	SD_CLK_P	SERDES REFERENCE CLOCK MINUS	SERDES Connector, Pin A13
A80	VCC3	3.3V OUTPUT	
B80	VCC3	3.3V OUTPUT	
A81	LV_CK_M	LVDS CLOCK MINUS	Remote Display I/F Connector P8, Pin B17
B81	LV_D2_M	LVDS DATA 2 MINUS	Remote Display I/F Connector P8, Pin B14
A82	LV_CK_P	LVDS CLOCK PLUS	Remote Display I/F Connector P8, Pin B16
B82	LV_D2_P	LVDS DATA 2 PLUS	Remote Display I/F Connector P8, Pin B13
A83	LCD_PWM	LCD BRIGHTNESS PWM CONTROL	Remote Display I/F Connector P8, Pin A8
B83	LCD_BKL	LCD BACKLIGHT POWER ENABLE	Remote Display I/F Connector P8, Pin A9
A84	LV_D1_M	LVDS DATA 1 MINUS	Remote Display I/F Connector P8, Pin B6
B84	LV_D0_M	LVDS DATA 0 MINUS	Remote Display I/F Connector P8, Pin B3
A85	LV_D1_P	LVDS DATA 1 PLUS	Remote Display I/F Connector P8, Pin B5
B85	LV_D0_P	LVDS DATA 0 PLUS	Remote Display I/F Connector P8, Pin B2
A86	GND	GROUND	
B86	GND	GROUND	
A87	PE2_TD_M	PCIe 2, TRANSMIT MINUS	PCIe Socket P16, Pin B20
B87	PE2_RD_M	PCIe 2, RECEIVE MINUS	PCIe Socket P16, Pin A22
A88	PE2_TD_P	PCIe 2, TRANSMIT PLUS	PCIe Socket P16, Pin B19
B88	PE2_RD_P	PCIe 2, RECEIVE PLUS	PCIe Socket P16, Pin A21
A89	PE1_DIR	PCIe 1 DIRECTION, 1 = Root Complex, 0 = Endpoint	Unconnected, Pulled Up on SOM
B89	*PE1_WAKE	PCIe 1 WAKEUP	PCIe Socket P16, Pin B11
A90	PE1_TD_M	PCIe 1, TRANSMIT MINUS	PCIe Socket P16, Pin B15
B90	PE1_RD_M	PCIe 1, RECEIVE MINUS	PCIe Socket P16, Pin A17
A91	PE1_TD_P	PCIe 1, TRANSMIT PLUS	PCIe Socket P16, Pin B14
B91	PE1_RD_P	PCIe 1, RECEIVE PLUS	PCIe Socket P16, Pin A16
A92	VCC3	3.3V OUTPUT	
B92	VCC3	3.3V OUTPUT	
A93	PE0_TD3_M	PCIe 0, LANE 3 TRANSMIT MINUS	PCIe Socket P18, Pin B28

PIN	NAME	DESCRIPTION	CSB1701 USAGE
B93	PE0_RD3_M	PCIe 0, LANE 3 RECEIVE MINUS	PCIe Socket P18, Pin A30
A94	PE0_TD3_P	PCIe 0, LANE 3 TRANSMIT PLUS	PCIe Socket P18, Pin B27
B94	PE0_RD3_P	PCIe 0, LANE 3 RECEIVE PLUS	PCIe Socket P18, Pin A29
A95	RSVD	RESERVED	
B95	RSVD	RESERVED	
A96	PE0_TD2_M	PCIe 0, LANE 2 TRANSMIT MINUS	PCIe Socket P18, Pin B24
B96	PE0_RD2_M	PCIe 0, LANE 2 RECEIVE MINUS	PCIe Socket P18, Pin A26
A97	PE0_TD2_P	PCIe 0, LANE 2 TRANSMIT PLUS	PCIe Socket P18, Pin B23
B97	PE0_RD2_P	PCIe 0, LANE 2 RECEIVE PLUS	PCIe Socket P18, Pin A25
A98	GND	GROUND	
B98	GND	GROUND	
A99	PE0_TD1_M	PCIe 0, LANE 1 TRANSMIT MINUS	PCIe Socket P18, Pin B20
B99	PE0_RD1_M	PCIe 0, LANE 1 RECEIVE MINUS	PCIe Socket P18, Pin A22
A100	PE0_TD1_P	PCIe 0, LANE 1 TRANSMIT PLUS	PCIe Socket P18, Pin B19
B100	PE0_RD1_P	PCIe 0, LANE 1 RECEIVE PLUS	PCIe Socket P18, Pin A21
A101	PE0_DIR	PCIe 0 DIRECTION, 1 = Root Complex, 0 = Endpoint	Unconnected, Pulled Up on SOM
B101	*PE0_WAKE	PCIe 0 WAKEUP	PCIe Socket P18, Pin B11
A102	PE0_TD0_M	PCIe 0, LANE 0 TRANSMIT MINUS	PCIe Socket P18, Pin B15
B102	PE0_RD0_M	PCIe 0, LANE 0 RECEIVE MINUS	PCIe Socket P18, Pin A17
A103	PE0_TD0_P	PCIe 0, LANE 0 TRANSMIT PLUS	PCIe Socket P18, Pin B14
B103	PE0_RD0_P	PCIe 0, LANE 0 RECEIVE PLUS	PCIe Socket P18, Pin A16
A104	GND	GROUND	
B104	GND	GROUND	
A105	VCC3	3.3V OUTPUT	
B105	VCC3	3.3V OUTPUT	
A106	IPM_SCL	IPM MICRO I2C BUS CLOCK	IPM ISP Header P5, Pin 3
B106	VIN	SOM POWER IN	+12V from ATX Power Supply
A107	IPM_SDA	IPM MICRO I2C BUS DATA	IPM ISP Header P5, Pin 4
B107	VIN	SOM POWER IN	+12V from ATX Power Supply
A108	*IPM_INT	IPM MICRO INTERRUPT	Unconnected

PIN	NAME	DESCRIPTION	CSB1701 USAGE
B108	VIN	SOM POWER IN	+12V from ATX Power Supply
A109	*IPM_RST	IPM MICRO RESET	IPM ISP Header P5, Pin 5
B109	VIN	SOM POWER IN	+12V from ATX Power Supply
A110	IPM_DBG	IPM MICRO DEBUG	IPM ISP Header P5, Pin 1
B110	VIN	SOM POWER IN	+12V from ATX Power Supply
A111	IPM_RFU	RESERVED FOR FUTURE IPM USE	Unconnected
B111	VIN	SOM POWER IN	+12V from ATX Power Supply
A112	FAN	CPU FAN CONTROL	Enable to FAN control circuit
B112	VIN	SOM POWER IN	+12V from ATX Power Supply
A113	TACH	CPU FAN SPEED	TACH from FAN control circuit
B113	VIN	SOM POWER IN	+12V from ATX Power Supply
A114	VCC3_SB	POWER TO IPM DEVICES	Output of 3.3V LDO VR1
B114	VIN	SOM POWER IN	+12V from ATX Power Supply
A115	RTC_BAT	RTC BATTERY BACKUP POWER	Coin Cell Holder B1
B115	VIN	SOM POWER IN	+12V from ATX Power Supply

Table 1 – CSB17xx MXM Connector Pin-Out

4 ON-BOARD DEVICES

4.1 INTRODUCTION

This section describes the various devices contained on the CSB1701

4.2 PCI EXPRESS CLOCK GENERATOR

An IDT ICS557-05 differential clock generator provides the 100Mhz differential reference clock required by the three PCIe sockets and the CSB17xx SOM.

4.3 4-PORT USB HUB

An SMSC Corp. USB2514 High Speed Four port hub is used to create additional USB Host Ports. The Upstream Port is fed from CSB17xx SOM USB Host Port 0. Hub Port 0 and 1 go to Ethernet/USB Combo Jack P7, while Hub Ports 2 and 3 go to Ethernet/USB Combo Jack P21.

4.4 USB TO SERIAL CONVERTER

A Microchip Technology Inc. MCP2200 is used to interface between a standard full speed (12Mbit/sec) USB Device port and the SOM UART 0 port. The MCP2200 presents to the host as a USB Virtual COM Port. Generic driver support is built into most versions of Windows and Desktop Linux. However, optimized drivers are available from the Microchip web site: <http://www.microchip.com>. As implemented on the CSB1701, the MCP2200 uses the default ID and configuration built into the chip.

5 CSB1701 CONNECTORS

5.1 OVERVIEW

This section provides the location and pin-outs of the various connectors, sockets, switches and indicators on the CSB1701.

5.2 CONNECTORS, HEADERS, SWITCHES AND LED LOCATIONS

Figure 2 - CSB1701 Connectors, Switches and LED Locations, shows the location of the various Connectors, Switches and LED's on the CSB1701.

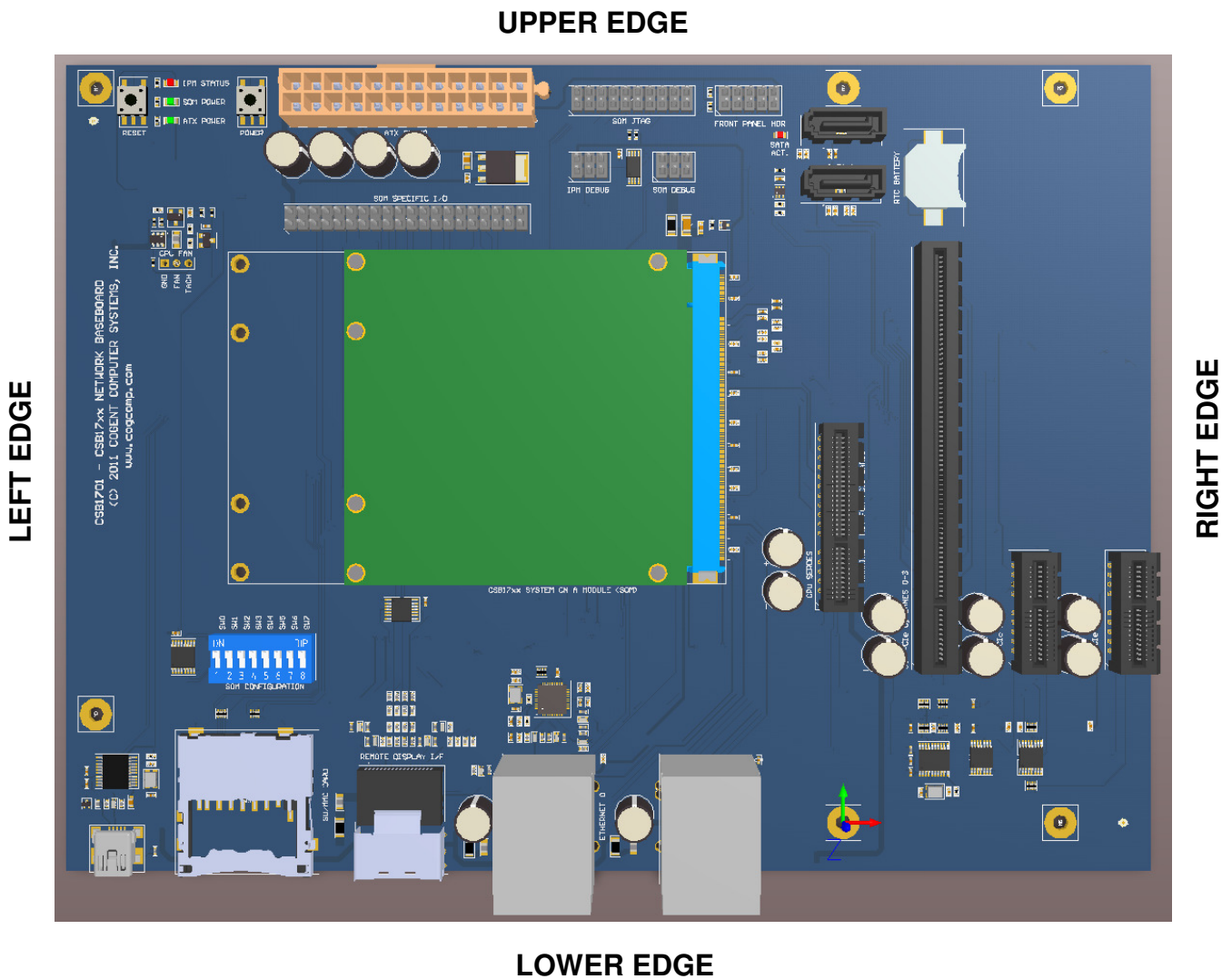


Figure 2 - CSB1701 Connectors, Switches and LED Locations

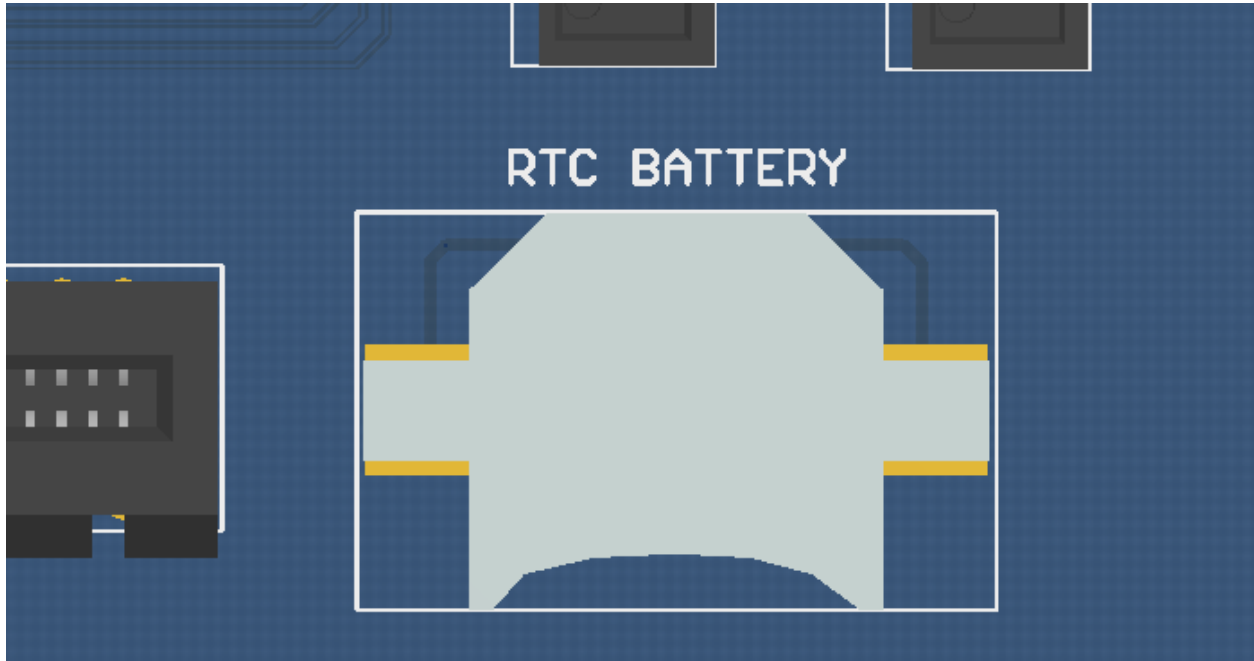


Figure 3 – Real Time Clock Battery Holder

5.1 B1 - REAL TIME CLOCK BATTERY HOLDER

B1, located near the upper right edge of the CSB1701, is used to hold a 3V, 12mm x 3mm, non-rechargeable coin cell. This cell provides backup power to the SOM RTC_BAT signal.



Figure 4 – P1 ATX Power Connector

5.1 P1 – 24-PIN ATX POWER CONNECTOR

P1 is a standard 24-Pin ATX style power connector located along the upper left edge of the CSB1701.

The pinout of this connector is shown in the following table.

Pin	Signal	Pin	Signal
1	+3.3V	13	+3.3V
2	+3.3V	14	-
3	GND	15	GND
4	+5V	16	*PS_ON
5	GND	17	GND
6	+5V	18	GND
7	GND	19	GND
8	PS_OK	20	-
9	+5V STBY	21	+5V
10	+12V	22	+5V
11	+12V	23	+5V
12	+3.3V	24	GND

Table 2 – P1 ATX Power Connector Pinout

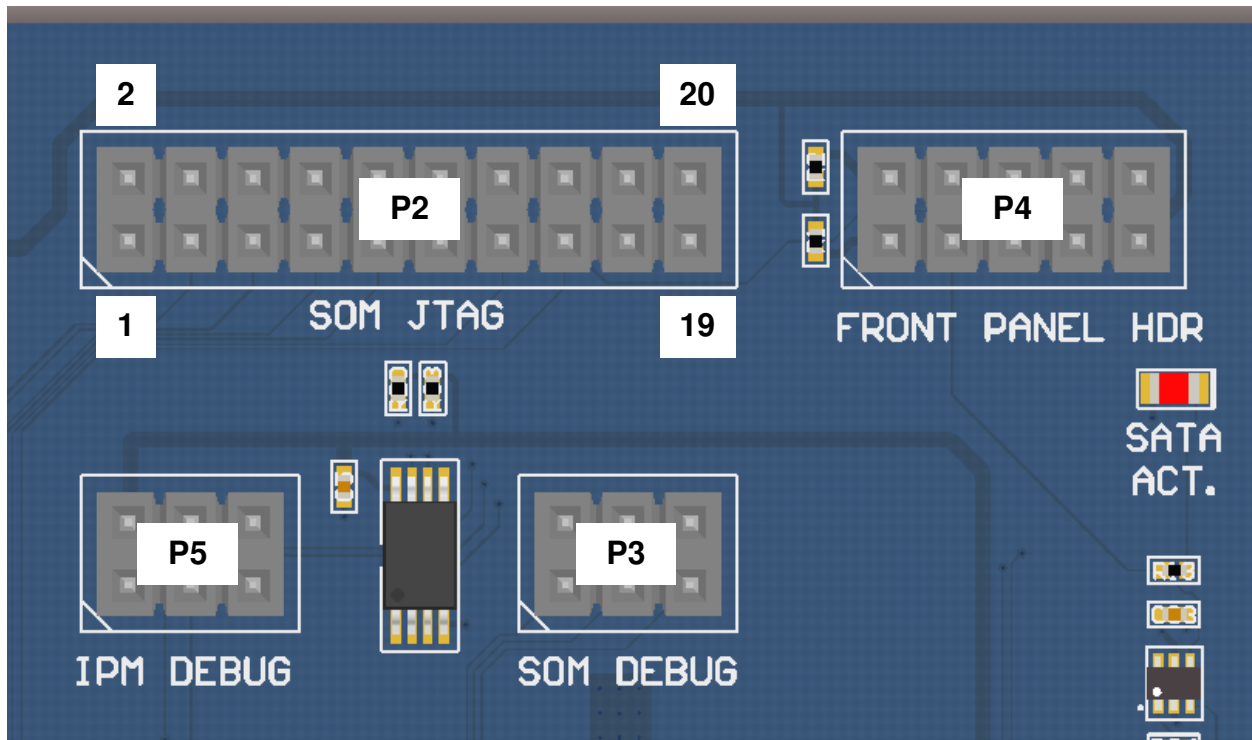


Figure 5 –Front Panel and Debug Headers

5.1 P2 – SOM JTAG HEADER

P2 is a 20-Pin, .1” Dual Row Header located near the upper middle edge of the CSB1701. It is used to connect to the SOM JTAG Port. The pinout is shown in the following table.

Pin	Signal	Pin	Signal
1	+3.3V	2	+3.3V
3	*TRST	4	GND
5	TDI	6	GND
7	TMS	8	GND
9	TCK	10	GND
11	-	12	GND
13	TDO	14	GND
15	*RST_IN	16	GND
17	-	18	GND
19	-	20	GND

Table 3 – P2 SOM JTAG Header Pinout

5.1 P3 – SOM DEBUG HEADER

P3 is a 6-Pin, .1” Dual Row Header located near the upper middle edge of the CSB1701. It provides access to any SOM specific debug signals to be used in conjunction with the JTAG port. Refer to the specific SOM for detailed use, if any, of these signals. The pinout is shown in the following table.

Pin	Signal	Pin	Signal
1	SOM_DBG0	2	GND
3	SOM_DBG0	4	GND
5	SOM_DBG0	6	GND

Table 4 – P3 SOM Debug Header Pinout

5.2 P4 – ATX FRONT PANEL HEADER

P4 is a 10-Pin, .1” Dual Row Header located near the upper middle edge of the CSB1701. It is used to connect the CSB1701 to typical ATX Case Front Panel Switches and Indicators. The pinout is shown in the following table.

Pin	Signal	Pin	Signal
1	HDD_LED +	2	PWR_LED +
3	HDD_LED -	4	PWR_LED -

Pin	Signal	Pin	Signal
5	RESET_SW	6	POWER_SW
7	GND	8	GND
9	+5V	10	-

Table 5 – P4 ATX Front Panel Header Pinout

5.1 P5 – IPM DEBUG HEADER

P5 is a 6-Pin, .1” Dual Row Header located near the upper left edge of the CSB1701. It provides access to the SOM IPM Micro debug/programming signals. This connector is for factory use only. The pinout is shown in the following table.

Pin	Signal	Pin	Signal
1	IPM_DBG	2	+3.3V STBY
3	IPM_SCL	4	IPM_SDA
5	*IPM_RST	6	GND

Table 6 – P5 IPM Debug Header Pinout

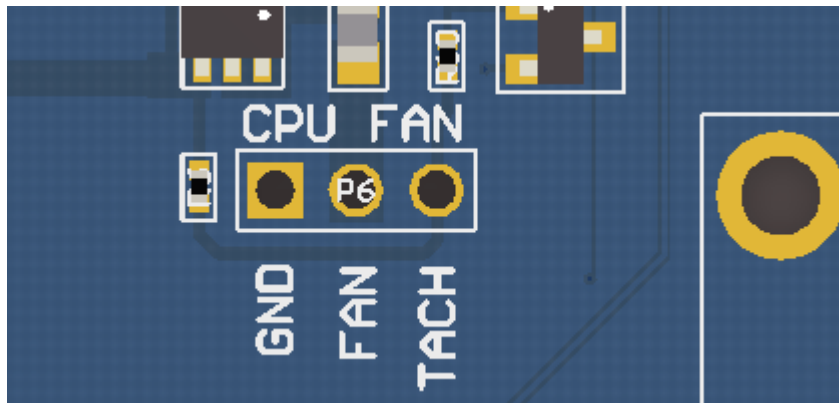


Figure 6 –SOM FAN Control Header

5.1 P6 –SOM FAN HEADER

P6 is an unpopulated 3-Pin, .1” Single Row Header located at the middle left of the CSB1701. It is designed to connect to a +12V fan with tachometer output. The circuitry on the CSB1701 is connected to the SOM IPM Micro Fan Control, if used. The pinout is shown in the following table.

Pin	Signal
1	GND
2	POWER

Pin	Signal
3	TACH

Table 7 – P6 SOM FAN Header Pinout

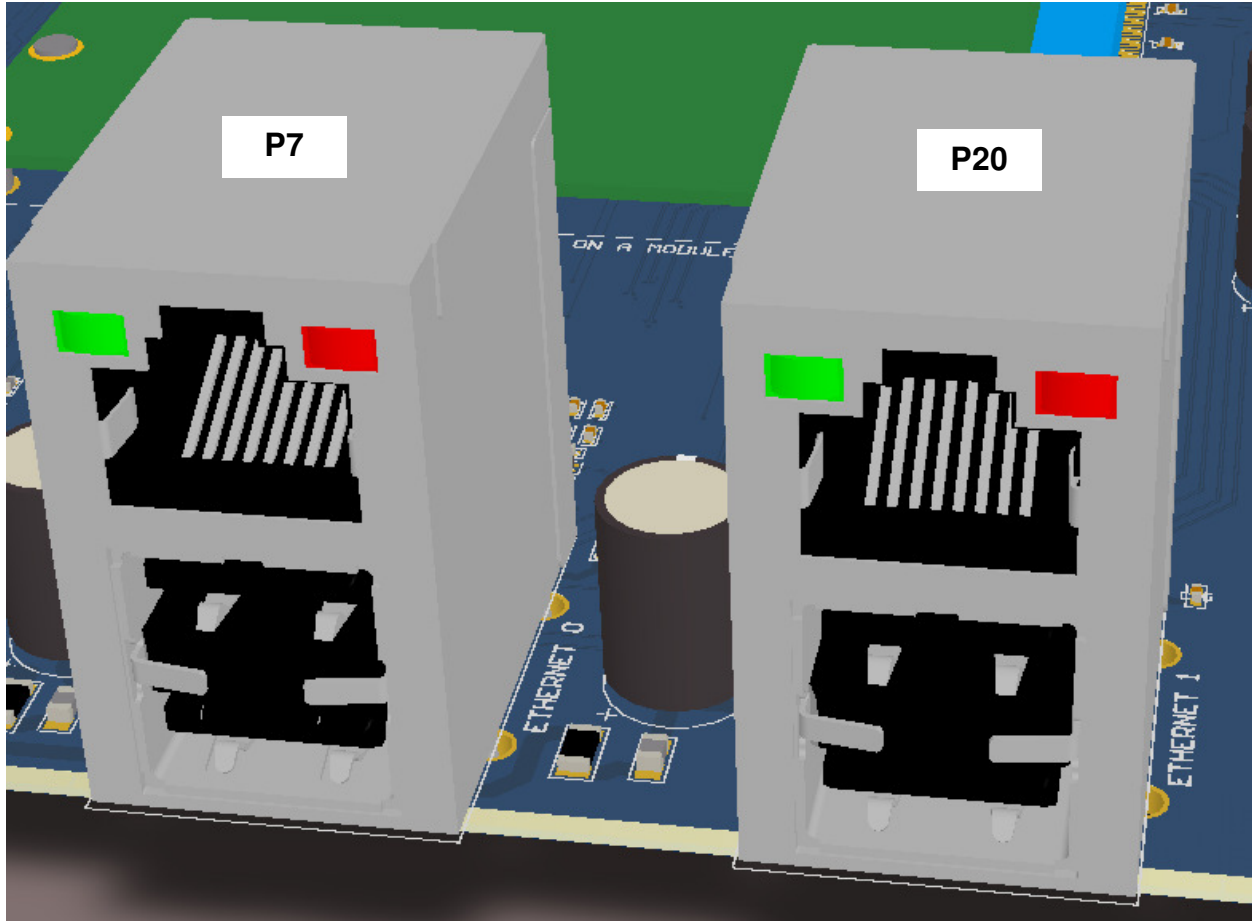


Figure 7 – P7 and P20 Combo USB/RJ45 Jacks

5.2 P7 AND P20 – COMBO USB/RJ45 JACK

P7 and P20 are combined RJ45 with Dual USB Type A stacked connectors located along the lower middle edge of the CSB1701. P7 connects to CSB17xx SOM 10/100/1000 port 0, USB Hub Port 0 (bottom) and USB Hub Port 1 (top). P20 connects to CSB17xx SOM 10/100/1000 port 1, CSB17xx SOM USB Hub Port 2 (bottom) and USB Hub Port 3 (top).

Each RJ45 section has two LED's. The Left LED is a Bi-Color Green/Orange LED and indicates connected speed (blank = 10mbit, Orange = 100Mbit, Green = 1000Mbit). The right LED is Yellow (or Red depending upon the actual jack that is installed) and is illuminated when a Link is active (regardless of speed). It also blinks off during transmit or receive activity.

Note that the LED behavior is assuming the corresponding CSB17xx SOM Ethernet PHY has been programmed correctly.

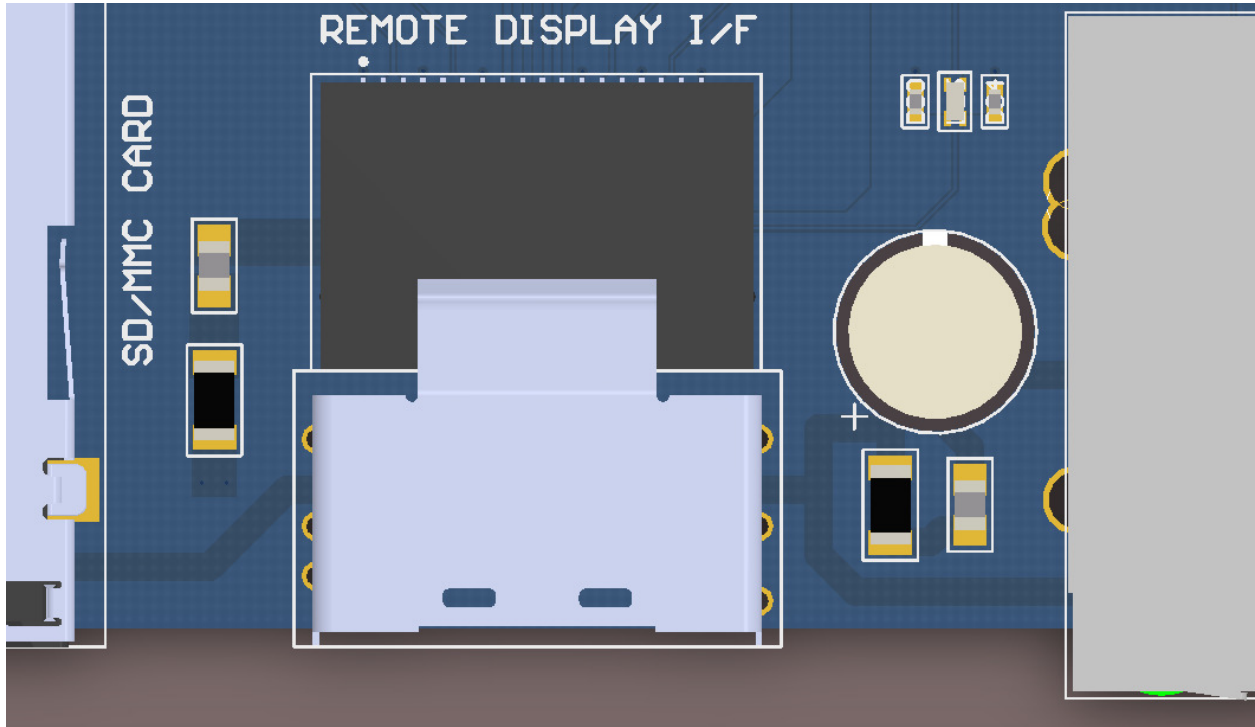


Figure 8 – P8 Remote Display I/F Connector – Top View



Figure 9 – P8 Remote Display I/F Connector – End View

5.1 P8 – REMOTE DISPLAY INTERFACE

P8 is a 36-Pin MINI-SAS connector, located along the lower middle edge of the CSB1701 that has been repurposed for use as a remote LCD display interface. It is designed to accept a standard type A Mini-SAS cable (SFF-8047). . The pinout is shown in the following table.

SIDE A	Name	SIDE B	Name
1	GND	1	GND
2	+12V	2	LV_D0_P
3	+12V	3	LV_D0_M
4	GND	4	GND
5	+12V	5	LV_D1_P
6	+12V	6	LV_D1_M
7	GND	7	GND
8	LCD_PWM	8	I2S_MCLK
9	LCD_BKL	9	I2S_BCLK
10	I2C1_SCL	10	I2S_LRCLK
11	I2C1_SDA	11	I2S_SDOUT
12	GND	12	GND
13	USB_DP	13	LV_D2_P
14	USB_DM	14	LV_D2_M
15	GND	15	GND
16	*RESET	16	LV_CK_M
17	*I2C_INT	17	LV_CK_P
18	GND	18	GND

Table 8 – P8 Remote Display I/F Connector Pinout

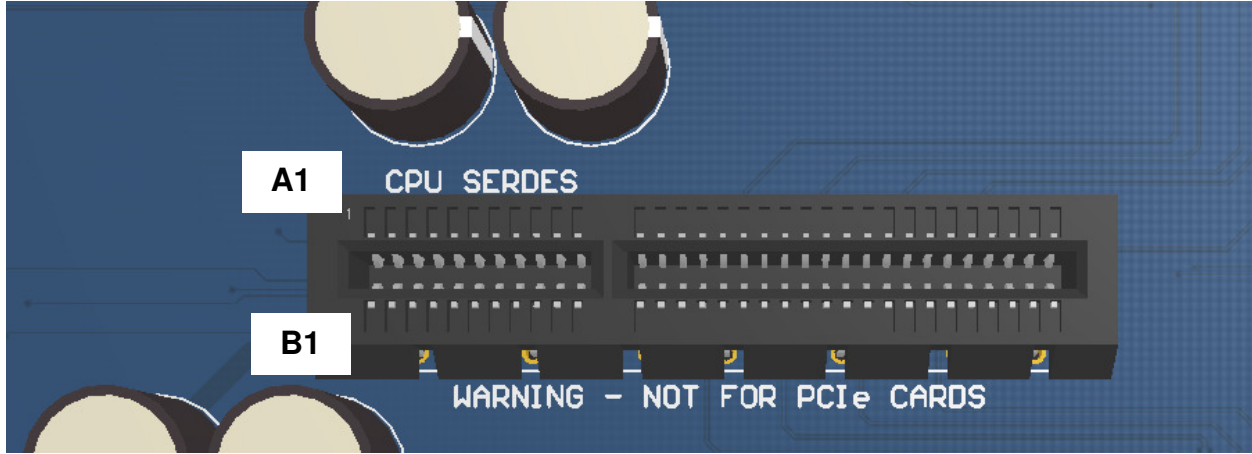


Figure 10 – P9 SOM SERDES Connector

5.1 P9 - SOM SPECIFIC SERDES CONNECTOR

P9 is a standard x4 PCIe connector, located at the lower right side of the CSB1701 that has been repurposed to provide access to any SOM specific SERDES (SGMII, XAUI, etc). It is set back from the standard mounting location to prevent inadvertent use with standard PCIe cards. The pinout is shown in the following table.

SIDE A	Name	SIDE B	Name
1	+12V	1	-
2	+12V	2	+12V
3	+12V	3	+12V
4	GND	4	GND
5	I2C_SCL	5	MDC
6	I2C_SDA	6	MDIO
7	GND	7	*MII_INT
8	+3.3V	8	-
9	-	9	+3.3V
10	+3.3V	10	+3.3V
11	*I2C_INT	11	*RESET
12	SD3_IO	12	GND
13	GND	13	SD_CK_M
14	SD3_RD_M	14	SD_CK_P
15	SD3_RD_P	15	GND
16	GND	16	SD3_TD_M

SIDE A	Name	SIDE B	Name
17	-	17	SD3_TD_P
18	GND	18	GND
19	SD1_RD_M	19	SD2_IO
20	SD1_RD_P	20	GND
21	GND	21	SD1_TD_M
22	GND	22	SD1_TD_P
23	SD2_RD_M	23	GND
24	SD2_RD_P	24	GND
25	GND	25	SD2_TD_M
26	GND	26	SD2_TD_P
27	SD0_RD_M	27	GND
28	SD0_RD_P	28	GND
29	GND	29	SD0_TD_M
30	SD1_IO	30	SD0_TD_P
31	-	31	GND
32	GND	32	SD0_IO

Table 9 – P9 SOM SERDES Connector Pinout

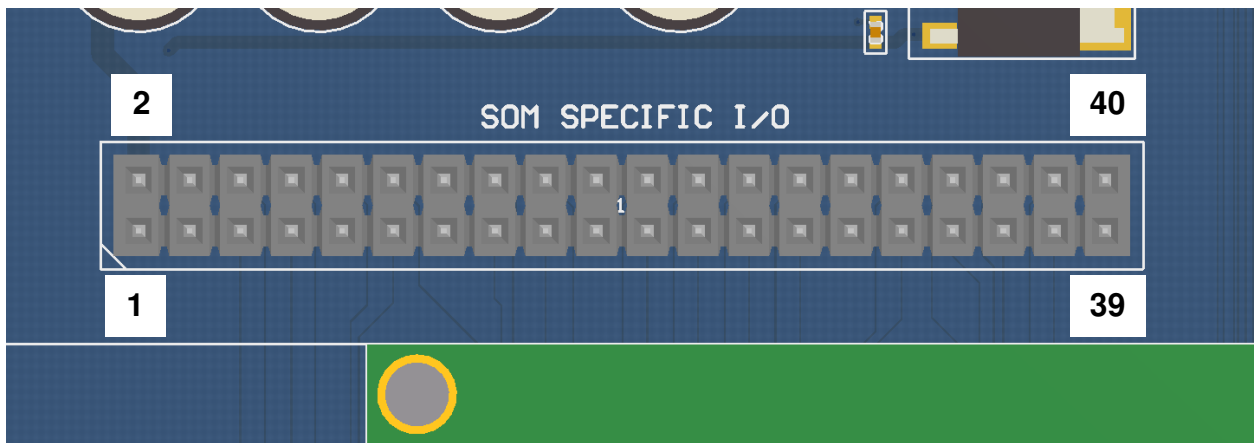


Figure 11 – P10 SOM I/O Expansion Connector

5.2 P10 - SOM SPECIFIC I/O CONNECTOR

P9 is a 40-Pin, .1" Dual Row Header located near the upper middle edge of the CSB1701. It is used to

connect to the various SOM I/O Ports. The pinout is shown in the following table.

P2 Pin	Signal	P2 Pin	Signal
1	+5V	2	+5V
3	+3.3V	4	+3.3V
5	*RST_OUT	6	I2C1_SCL
7	I2C1_SDA	8	*I2C_INT
9	-	10	I2S_MCLK
11	SSI_RDY	12	SSI_MCLK
13	GND	14	GND
15	I2S_BCLK	16	I2S_LRCLK
17	I2S_SDOOUT	18	I2S_SDIN
19	GND	20	GND
21	SSI_TXD	22	SSI_RXD
23	SSI_CLK	24	SSI_SYNC
25	SPI_MOSI	26	SPI_MISO
27	SPI_CLK	28	SPI_CS
29	-	30	GND
31	U2_TXD	32	U2_RXD
33	U2_RTS	34	U2_CTS
35	U1_TXD	36	U1_RXD
37	U1_RTS	38	U1_CTS
39	GND	40	GND

Table 10 – P9 SOM I/O Expansion Connector Pinout

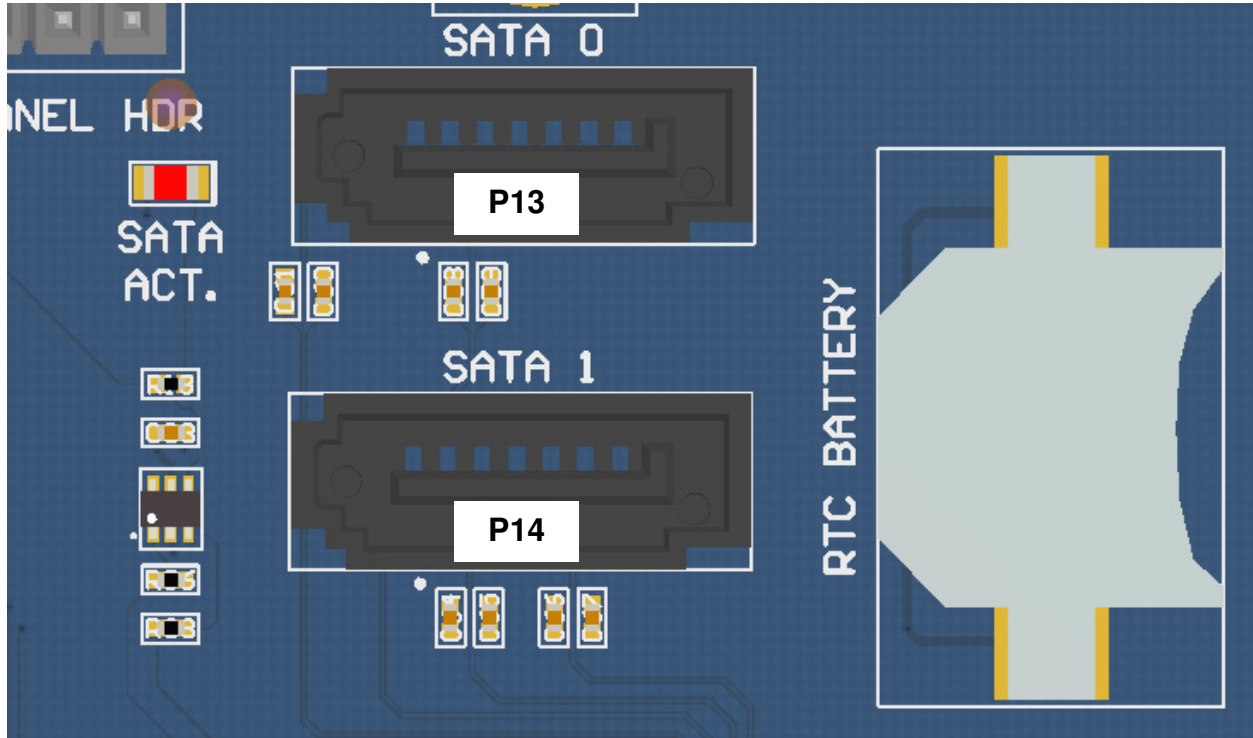


Figure 12 – P13 and P14 SATA Connectors

5.3 P13 AND P14 – SATA CONNECTORS

P13 and P14 are industry standard 7-Pin SATA connectors located near the upper right edge of the CSB1701. They provide access to the CSB17xx SOM SATA Ports 0 and 1 respectively. RED LED D13 is active when either SATA channel is active.

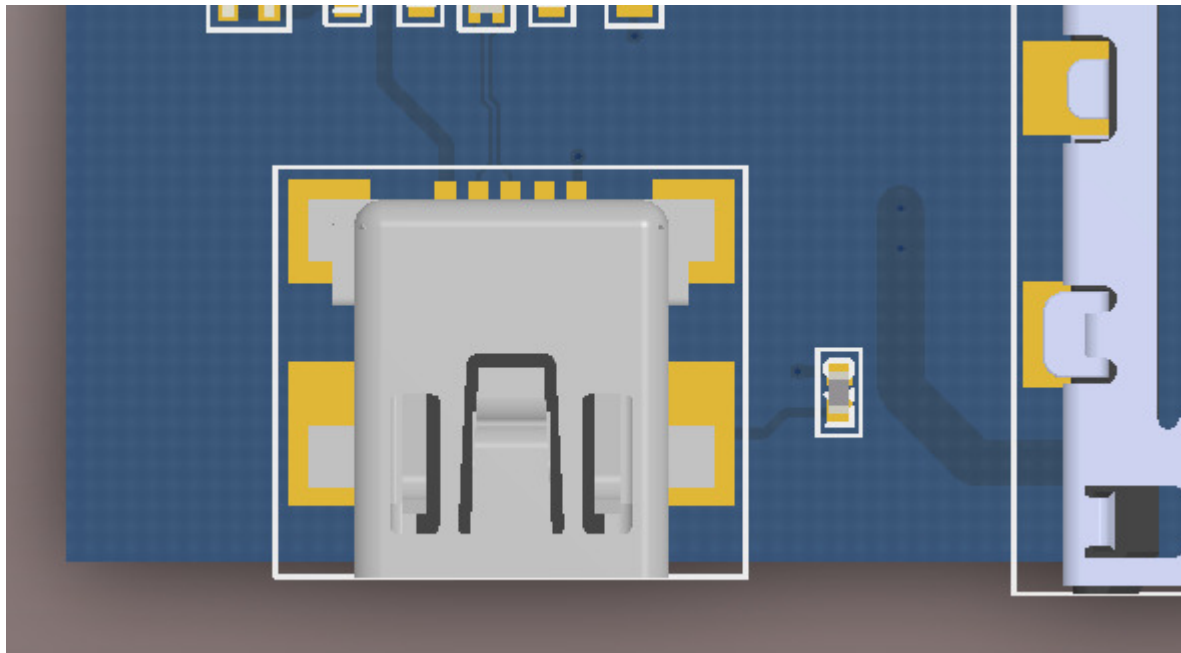


Figure 13 – P15 USB Serial Connector

5.1 P15 - USB SERIAL CONNECTOR

P15 is an industry standard USB Mini-B Connector located along the lower left edge of the CSB1701. It interfaces with the MCP2200 USB to Serial Converter. It is used to provide a console I/O port for SOM UART 0.

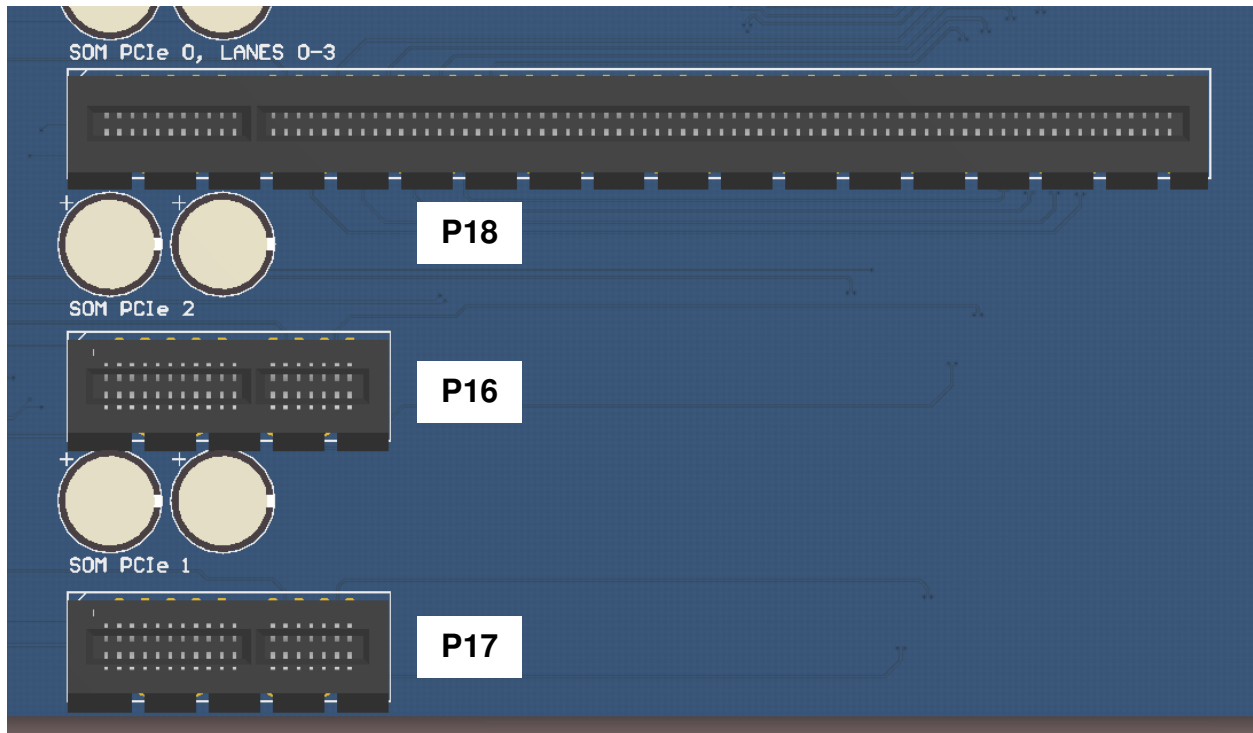


Figure 14 – P16, P17 and P18 PCI Express Connectors

5.2 P16 – X1 PCI EXPRESS CONNECTOR

P16 is an industry standard x1 PCI Express Connector located near the lower right edge of the CSB1701. CSB17xx PCIe Port 1 is routed to P16. Support for this port is SOM specific. CSB17xx SOM I2C0_SDA and I2C0_SCL are routed to P16 I2C_SDA and I2C_SCL respectively. The Wake signal from P16 is routed to SOM signal *WAKE1.

5.3 P17 – X1 PCI EXPRESS CONNECTOR

P17 is an industry standard x1 PCI Express Connector located near the lower right edge of the CSB1701. CSB17xx PCIe Port 1 is routed to P17. Support for this port is SOM specific. CSB17xx SOM I2C0_SDA and I2C0_SCL are routed to P17 I2C_SDA and I2C_SCL respectively.

5.4 P18 – X16 PCI EXPRESS CONNECTOR

P18 is an industry standard x16 PCI Express Connector located near the lower right edge of the CSB1701. CSB17xx PCIe Port 0, Lanes 0-3 are routed to P18, supporting x1, x2 or x4 operation.

Support and width for this port is SOM specific. CSB17xx SOM I2C0_SDA and I2C0_SCL are routed to P18 I2C_SDA and I2C_SCL respectively. The Wake signal from P18 is routed to SOM signal *WAKE0.

5.1 P21 – CSB17XX MXM CONNECTOR

P1 is a 230-Pin MXM Type II Connector. Pinout of this connector is fully described in Section 3.

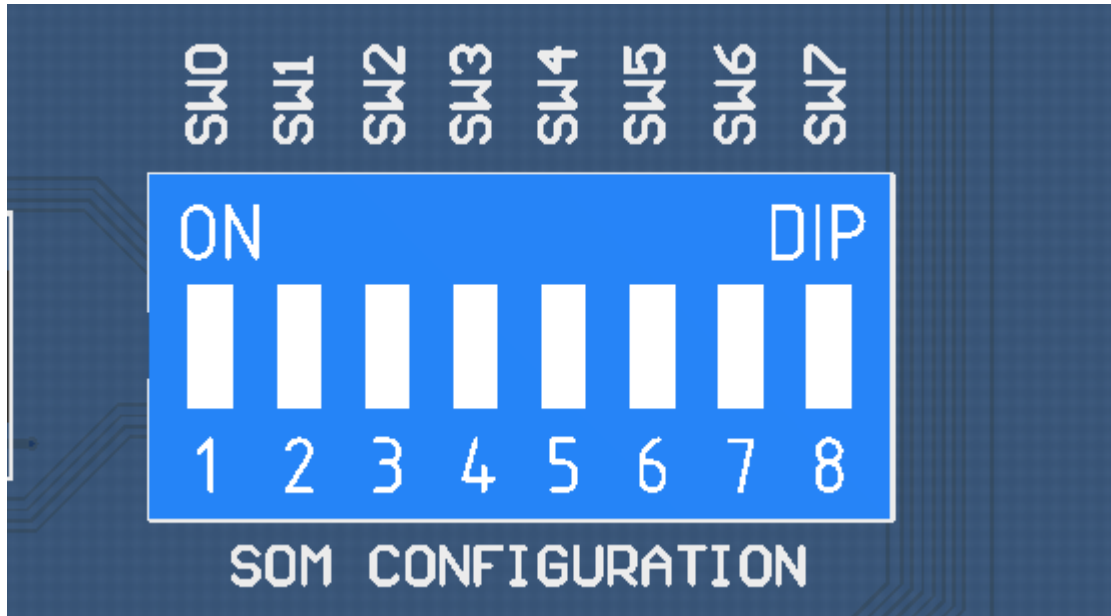


Figure 15 – SOM Configuration DIP Switch

5.1 SW1 - SOM CONFIGURATION DIP SWITCH

SW1 is an 8 position dip switch just above the SD/MMC Card socket. It is read by the SOM IPM Micro to set various options prior to boot. Refer to the SOM documentation for the SOM Specific meaning of each of these switches.

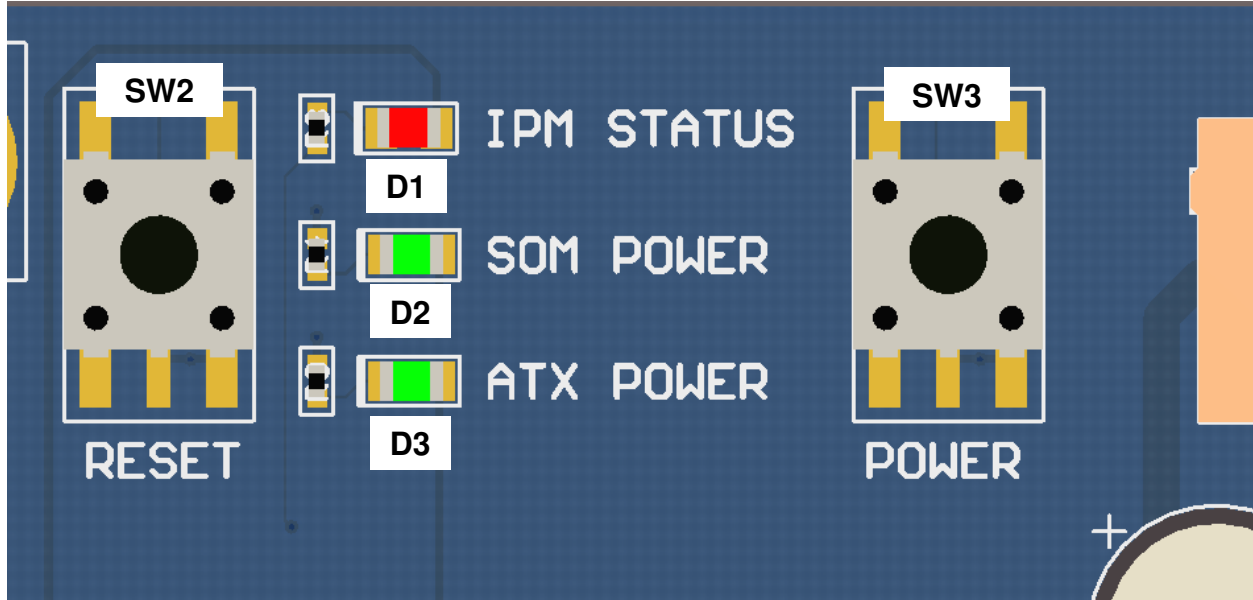


Figure 16 – Pushbutton Switches and LED Indicators

5.2 SW2 AND SW3 - PUSHBUTTON SWITCHES

There are two Push Button switches located near the left upper edge of the CSB1701. SW2, when pressed, drives the CSB17xx SOM *RST_IN signal low. SW3, when pressed, will drive the CSB17xx IPM *PWR_SW signal low. These are identical to the front panel header signals and are provided for convenience when the CSB1701 is operated outside of an ATX case.

5.3 INDICATOR LED'S

There are three LED's located near the top left edge of the CSB1701. D3 is a Green LED powered from the ATX Power Supply +5V rail and is illuminated when the ATX Power Supply is turned on. D2 is a Green LED powered from the SOM +3.3V rail (this is separate from the ATX +3.3V rail). It is on when the SOM is powered up. D1 is a Red LED driven by the IPM Micro. It is on when the SOM is in standby or when an internal error has been detected by the IPM Micro.

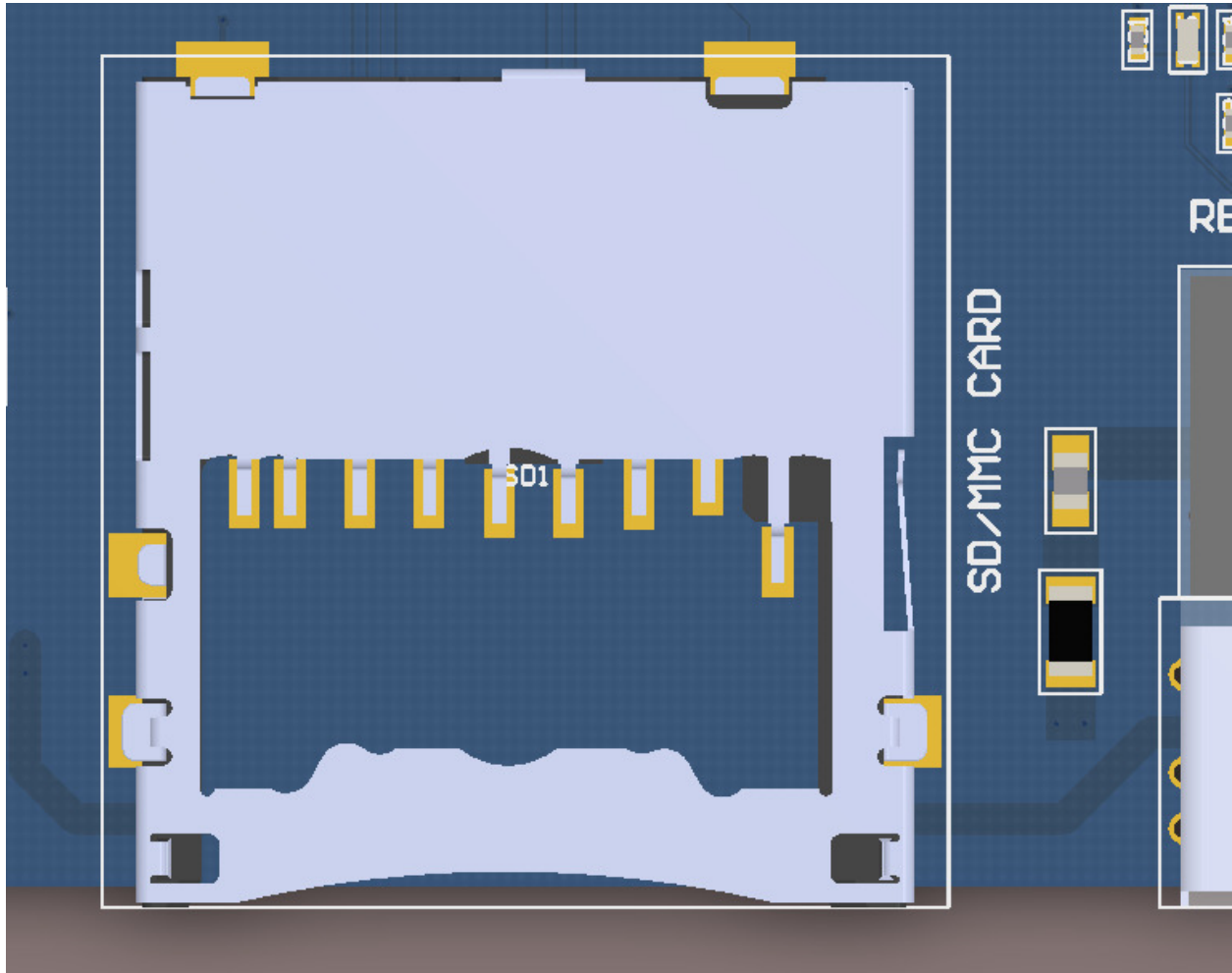


Figure 17 – SD/MMC Card Socket

5.1 SD1 - SD/MMC CARD SOCKET

SD1 is a standard full size SD/MMC Card Socket. This socket is located on the bottom left edge. Support is SOM Specific.

6 DOCUMENT REVISIONS

Date	Revision	Change
8/22/2011	P2.0	First Release for CSB1701 Rev. P2 (No Rev. P1)

Table 11 – Document Revisions